

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of Gerhard Enders et al.

Serial No.: Not Yet Assigned

Filed: Herewith

For: Integrated Semiconductor Memory with a Selection Transistor Formed at a Web

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §1.97(b)**

Pursuant to the duty imposed by 37 C.F.R. §1.56 to disclose information which may be material to the patentability of the above-identified patent application, the Applicants would like to direct the Examiner's attention to the documents listed on the enclosed Information Disclosure Citation Form (PTO/SB/08). In accordance with this duty of disclosure, Applicants hereby submit the following information in conformance with 37 C.F.R. §§1.97 and 1.98.

- ☐ Pursuant to 37 C.F.R. §1.98, a copy of each document cited in the attached Form PTO/SB/08 is enclosed.
- ☒ The subject Information Disclosure Statement is being filed without copies of the listed U.S. Patents and/or U.S. patent application publications pursuant to the waiver of the requirement under 37 C.F.R. §1.98(a)(2)(i) for applications filed after June 30, 2003. Copies of the listed foreign patent documents and/or non-patent literature are enclosed herewith.
- ☐ No copies of the publications listed on the attached Form PTO/SB/08A are being provided pursuant to 37 C.F.R. §1.98(d) because the publications were previously cited by or submitted to the Office in prior Application Serial No. _____ to which the above-identified application claims priority under 35 U.S.C. §120.
- ☐ Publication(s) _____ listed on the attached Form PTO/SB/08A were cited in a foreign search or examination report corresponding to _____ application serial no. _____ and mailed on _____.

- ☐ Enclosed is a copy of a non-English publication(s) _____. Pursuant to §609 of the M.P.E.P., Applicant submits the attached foreign search or examination report, which cites such non-English language publication(s).
- ☒ Enclosed is a copy of a non-English publication DE 3640363A1.
- ☒ Enclosed is an English Abstract of non-English publication DE 3640363A1 for which an English translation is not available.
- ☐ Enclosed is an English translation of the non-English publication(s) cited in the attached Form PTO/SB/08A.
- ☐ Enclosed is a copy of pending patent Application Serial No. _____.

This Information Disclosure Statement is filed within any one of the following time periods:

- ☐ within three months from the filing date of this national application other than a CPA under 37 C.F.R. § 1.53(d);
- ☐ within three months from the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in this international application;
- ☒ before the mailing date of a first office action on the merits; or
- ☐ before the mailing of a first office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

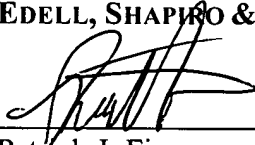
It is respectfully requested that the Examiner consider the above-noted information and return an initialed copy of the attached Form PTO/SB/08A to the undersigned.

Dated: December 5, 2003

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Respectfully submitted by
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PTO/SB/08A (08-00)

Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	Herewith
				First Named Inventor	Gerhard Enders et al.
				Group Art Unit	Unknown
				Examiner Name	Unknown
Sheet	2	of	2	Attorney Docket Number	0928.0006C

OTHER DOCUMENTS – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
		YANG-KYU CHOI ET AL., Sub-20nm CMOS FinFet Technologies, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, 2001, 4 pages.		

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number.

² Applicant is to place a check mark here if English language Translation attached.

PURPOSE: To provide the titled memory with an excavated capacitor structure extremely resistant to any soft errors eliminating any deep grooves and facilitating the formation by a method wherein a capacitor electrode to be a memory node and an MOS transistor are formed on a semiconductor substrate through the intermediary of an insulating film.

CONSTITUTION: Capacitor forming grooves 2 are formed on specified positions on a P-type silicon substrate 1 by reactive ion etching process and after forming a thermal oxide film and depositing a polycrystalline silicon film 4 to be etched, patterns are formed on multiple rectangular island regions. Later, the silicon film 4 is single crystallized and the part buried in the grooves 2 are doped with an impurity to form N+ type layers as capacitor electrodes 5. Next, thermal oxide films as gate insulating films 6 are formed; the second polycrystalline silicon films are deposited; and after these films are patterned to form gate electrodes 7, an N+ type source region 81 and a drain region 82 are formed by ion implantation. Finally, a CVD insulating film 9 is deposited on overall surface to make a contact hole 11 forming an Al interconnection 10.